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IEEE JNL IEEE Journal or

Magazine

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IEEE CNF | IEEE Conference

Proceeding

IEE CNF IEE Conference

Proceeding

IEEE STD IEEE Standard

1. Using incorrect speculation to prefetch data in a concurrent multithreaded processor

Ying Chen; Sendag, R.; Lija, D.J.

Parallel and Distributed Processing Symposium, 2003. Proceedings. International

22-26 April 2003

Page(s): 9 pp.-

Digital Object Identifier 10.1109/IPDPS.2003.1213177

Summary: Concurrent multithreaded architectures exploit both instruction-level and thread-level parallelism through a combination of branch prediction and thread-level control speculation. The

resulting speculative issuing of load instructions in these archi.....

AbstractPlus | Full Text: PDF | IEEE CNF

2. Accurate modeling of aggressive speculation in modern microprocessor architectures

Modi, H.; Spracklen, L.; Chou, Y.; Abraham, S.G.

Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, 2005. 13th IEEE

International Symposium on

27-29 Sept. 2005

Page(s): 75-84

Digital Object Identifier 10.1109/MASCOTS.2005.12

Summary: Computer architects utilize cycle simulators to evaluate microprocessor chip design tradeoffs and estimate performance metrics. Traditionally, cycle simulators are either trace-driven or

execution-driven. In this paper, we describe ValueSim, a softw.....

AbstractPlus | Full Text: PDF | IEEE CNF

An analysis of the performance impact of wrong-path memory references on out-of-ord r and runahead execution processors

Mutlu, O.; Kim, H.; Armstrong, D.N.; Patt, Y.N.

Computers, IEEE Transactions on Volume: 54 Issue: 12 Dec. 2005

Page(s): 1556- 1571

Digital Object Identifier 10.1109/TC.2005.190

Summary: High-performance, out-of-order execution processors spend a significant portion of their execution time on the incorrect program path even though they employ aggressive branch prediction algorithms. Although memory references generated on the wrong

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